

Environment Completeness



Verification Leadership Seminar - June 2008

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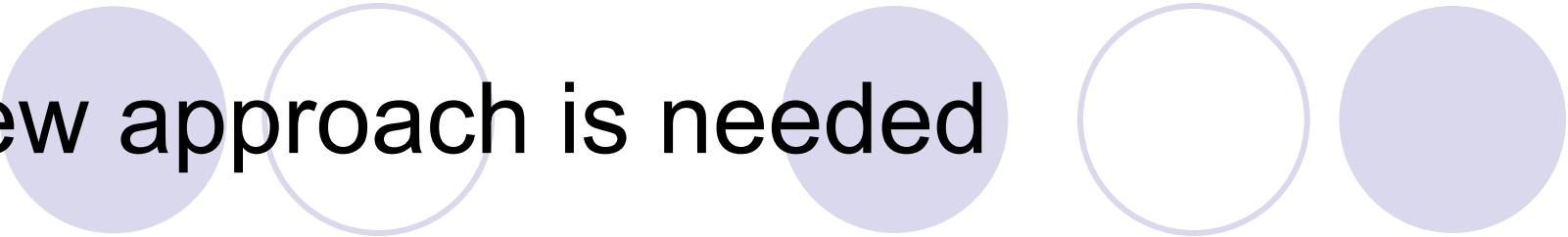
When VE is complete?

A naive answer might be:

- When the VE generates all inputs possible:
 - Driving all input signals permutations
 - generating all the signals transactions
- When the VE “knows” to check all outputs.

The problem is?

- Its almost not feasible (for large designs)
 - How do I know the VE does generate all required inputs
 - How do I know to generate valid content
 - How do I know when the VE is complete
 - It takes too long to simulate
- Checking the outputs:
 - How do I know what to expect
 - How do I know when to expect outputs
 - How deep to go into the DUT



New approach is needed

- We can use a higher level of abstraction
- We can use coverage to set goals for the interesting scenarios
- We can use random generation to create the different inputs
- But still we do not have a methodology for completeness of the VE

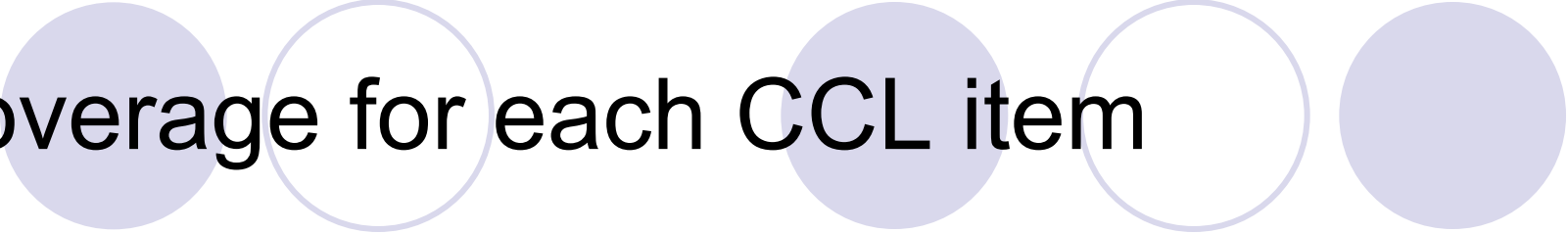
CCL in the Verification Plan

- Rules extraction from the specification
 - A File that contains all the rules from the spec – Compliance Check List (CCL)
 - Specification rules can be implied also by diagrams and tables
 - Beware of implicit assumptions.

Creating the Checkers in the VE

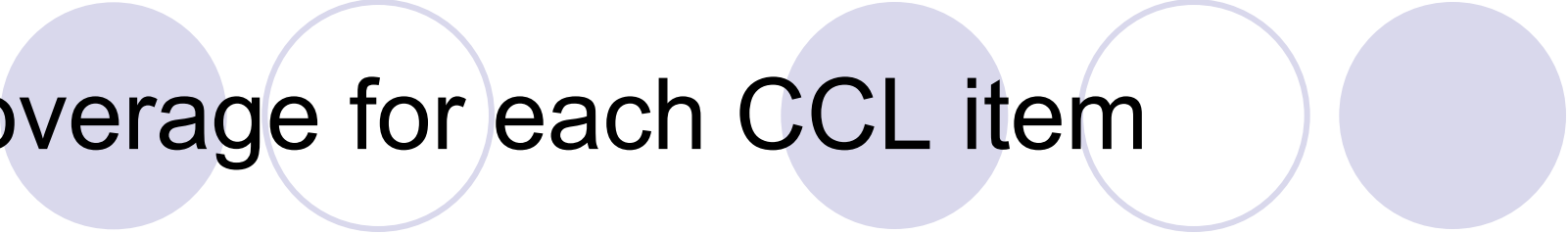
- Checker for each Compliance Check List item.
 - This checker should issue an error if the Device Under Test (DUT) violated one of the identified rules.
 - For example:
 - check that `(pkt.len <= 20)` else `dut_error "DUT error 0001: packet must be shorter or equal to 20 bytes";`

Coverage for each CCL item



- Go over the vPlan Compliance Checks and define for each one of them the relevant coverage.
 - Subjective operation
 - Not to large
 - Not to small

Coverage for each CCL item



- Easy to find holes in the defined coverage
- Working in small scales
- Easy to maintain and modify when the spec changes
- Easy to criticize

Test Suite



- The power to create all the interesting scenarios
- Test Suite goal is to get to 100% of the Verification plan coverage

Last words...

